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AK4524
24Bit 96kHz Audio CODEC

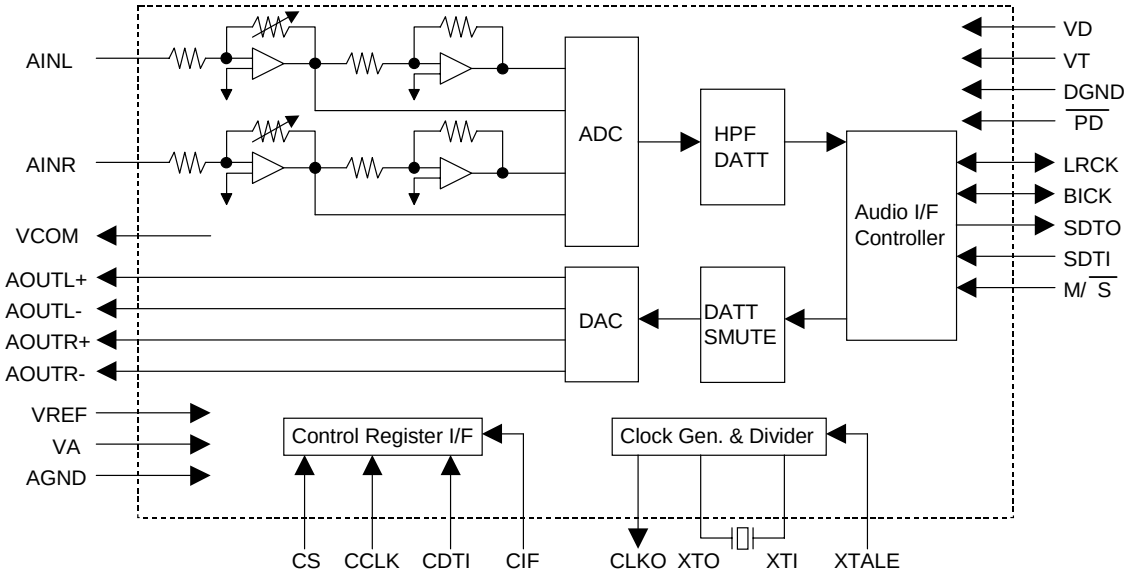
GENERAL DESCRIPTION

The AK4524 is a high performance 24bit CODEC for the 96kHz recording system. The ADC has an Enhanced Dual Bit architecture with wide dynamic range. The DAC uses the new developed Advanced Multi Bit architecture and achieves low outband noise and high jitter tolerance by use of SCF (switched capacitor filter) techniques. The AK4524 has an input PGA and is well suited MD, DVTR system and musical instruments.

FEATURES

- **24bit 2ch ADC**
  - **64x Oversampling**
  - **Single-End Inputs**
  - **S/(N+D): 90dB**
  - **Dynamic Range, S/N: 100dB**
  - **Digital HPF for offset cancellation**
  - **Input PGA with +18dB gain & 0.5dB step**
  - **Input DATT with -72dB att**
  - **I/F format: MSB justified or I^2S**
- **24bit 2ch DAC**
  - **128x Oversampling**
  - **24bit 8 times Digital Filter**
    Ripple: ±0.005dB, Attenuation: 75dB
  - **SCF**
  - **Differential Outputs**
  - **S/(N+D): 94dB**
  - **Dynamic Range, S/N: 110dB**
  - **De-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
  - **Output DATT with -72dB att**
  - **Soft Mute**
  - **I/F format: MSB justified, LSB justified or I^2S**
- **High Jitter Tolerance**
- **3-wire Serial Interface for Volume Control**
- **Master Clock**
  - **X'tal Oscillating Circuit**
  - **256fs/384fs/512fs/768fs/1024fs**
- **Master Mode/Slave Mode**
- **5V operation**
- **3V Power Supply Pin for 3V I/F**
- **Small 28pin VSOP package**

■ Block Diagram

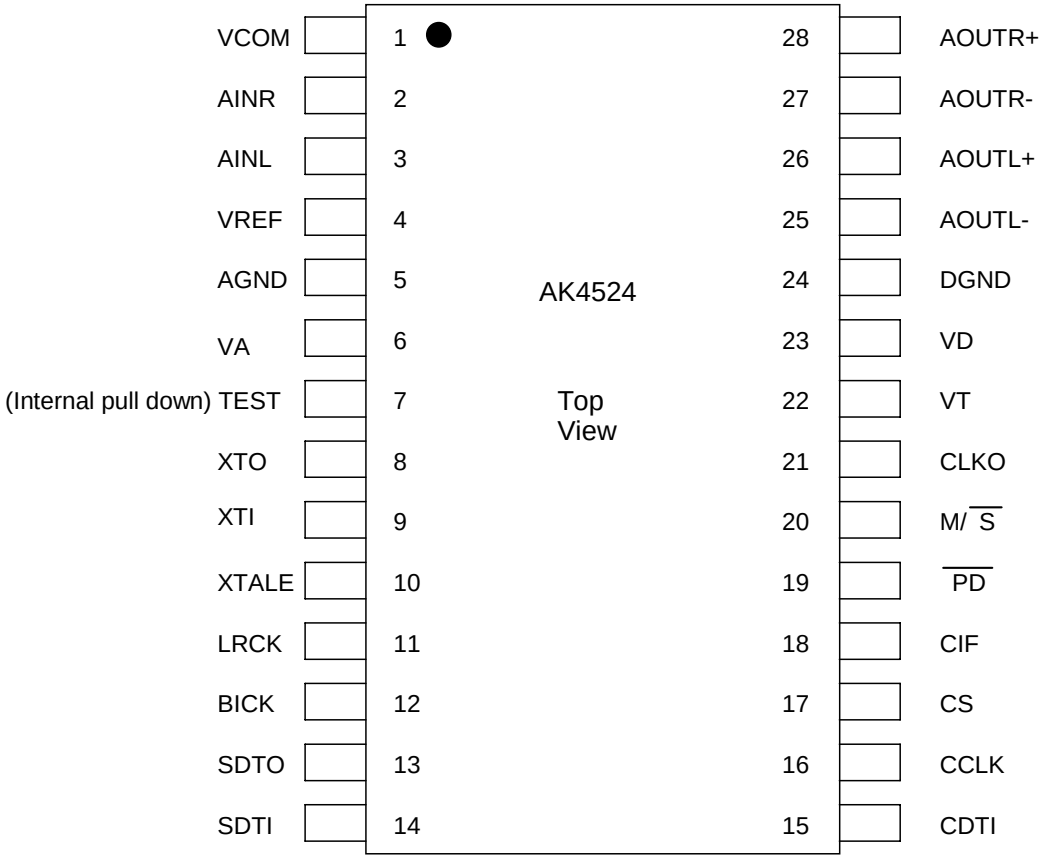


Block Diagram

■ Ordering Guide

AK4524VF	-10~+70°C	28pin VSOP (0.65mm pitch)
AKD4524	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, VA/2 Bias voltage of ADC inputs and DAC outputs.
2	AINR	I	Rch Analog Input Pin
3	AINL	I	Lch Analog Input Pin
4	VREF	I	Voltage Reference Input Pin, VA Used as a voltage reference by ADC & DAC. VREF is connected externally to filtered VA.
5	AGND	-	Analog Ground Pin
6	VA	-	Analog Power Supply Pin, 4.75 ~ 5.25V
7	TEST	I	Test Pin (Internal pull-down pin)
8	XTO	O	X'tal Output Pin
9	XTI	I	X'tal/Master Clock Input Pin
10	XTALE	I	X'tal Osc Enable Pin "H": Enable, "L": Disable
11	LRCK	I/O	Input/Output Channel Clock Pin
12	BICK	I/O	Audio Serial Data Clock Pin
13	SDTO	O	Audio Serial Data Output Pin
14	SDTI	I	Audio Serial Data Input Pin
15	CDTI	I	Control Data Input Pin
16	CCLK	I	Control Data Clock Pin
17	CS	I	Chip Select Pin
18	CIF	I	Control Data I/F Format Pin "H": CS falling trigger, "L": CS rising trigger
19	$\overline{PD}$	I	Power-Down Mode Pin "H": Power up, "L": Power down, reset and initialize the control register.
20	M/$\overline{S}$	I	Master/Slave Mode Pin "H": Master mode, "L": Slave mode
21	CLKO	O	Master Clock Output Pin
22	VT	-	Output Buffer Power Supply Pin, 2.7 ~ 5.25V
23	VD	-	Digital Power Supply Pin, 4.75 ~ 5.25V
24	DGND	-	Digital Ground Pin
25	AOUTL-	O	Lch Negative Analog Output Pin
26	AOUTL+	O	Lch Positive Analog Output Pin
27	AOUTR-	O	Rch Negative Analog Output Pin
28	AOUTR+	O	Rch Positive Analog Output Pin

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Output Buffer	VT	-0.3	6.0	V
	VD-VA	VDA	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VA+0.3	V
Ambient Temperature (powered applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note:1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	4.75	5.0	5.25	V
(Note 2)	Digital	VD	4.75	5.0	VA	V
	Output Buffer	VT	2.7	3.0	VD	V
Voltage Reference		VREF	3.0	-	VA	V

Note:1. All voltages with respect to ground.
2. VA and VD should be powered at the same time or VA should be powered earlier than VD.
The power up sequence between VA and VT, or VD and VT is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD, VT=5.0V; AGND=DGND=0V; VREF=VA; fs=44.1kHz; Signal Frequency =1kHz; 24bit Data; Measurement frequency = 10Hz ~ 20kHz at fs=44.1kHz, 10Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Input PGA Characteristics:					
Input Voltage (Note 3)		2.7	2.9	3.1	Vpp
Input Resistance		5	10	15	kΩ
Step Size		0.2	0.5	0.8	dB
Gain Control Range		0		18	dB
ADC Analog Input Characteristics: IPGA=0dB					
Resolution				24	Bits
S/(N+D) (-0.5dBFS)	fs=44.1kHz fs=96kHz	84 80	90 88		dB dB
DR (-60dBFS)	fs=44.1kHz, A-weighted fs=96kHz	94 88	100 96		dB dB
S/N	fs=44.1kHz, A-weighted fs=96kHz	94 88	100 96		dB dB
Interchannel Isolation		90	105		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Power Supply Rejection (Note 4)			50	-	dB
DAC Analog Output Characteristics:					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=44.1kHz fs=96kHz	88 85	94 93		dB dB
DR (-60dBFS)	fs=44.1kHz, A-weighted fs=96kHz	104 96	110 104		dB dB
S/N	fs=44.1kHz, A-weighted fs=96kHz	104 96	110 104		dB dB
Interchannel Isolation		100	110		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage (Note 5)		5.0	5.4	5.8	Vpp
Load Resistance (In case of AC load)		1			kΩ
Output Current (In case of AC load)				1.5	mA
Load Capacitance				25	pF

Note: 3. Full scale (0dB) of the input voltage at PGA=0dB.
This voltage is proportional to VREF. Vin=0.58 x VREF.
4. PSR is applied to VA, VD, VT with 1kHz, 50mVpp. VREF pin is held a constant voltage.
5. Full scale (0dB) of the output voltage when summing the differential outputs, AOUT+/- by unity gain.
This voltage is proportional to VREF. Vout=1.08 x VREF x Gain.

Parameter	min	typ	max	Units
Power Supplies				
Power Supply Current				
Normal Operation ($\overline{PD}$ = "H")				
VA		30	45	mA
VD+VT (fs=44.1kHz)		16	24	mA
(fs=96kHz)		24	36	mA
Power-down mode ($\overline{PD}$ = "L") (Note 6)				
VA		10	100	uA
VD+VT		10	100	uA

Note: 6. XTALE="L" and all digital input pins are held VD or DGND.

FILTER CHARACTERISTICS

(Ta=25°C; VA, VD=4.75 ~ 5.25V; VT=2.7 ~ 5.25V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 7)	-0.005dB	PB	0		19.76	kHz
	-0.02dB		-	20.02	-	kHz
	-0.06dB		-	22.20	-	kHz
	-6.0dB		-	22.05	-	kHz
Stopband		SB	24.34			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 8)		GD		31		1/fs
Group Delay Distortion		ΔGD		0		us
ADC Digital Filter (HPF):						
Frequency Response (Note 5)	-3dB	FR		0.9		Hz
	-0.5dB			2.7		Hz
	-0.1dB			6.0		Hz
DAC Digital Filter:						
Passband (Note 7)	-0.01dB	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 8)		GD		30		1/fs
DAC Digital Filter + SCF:						
Frequency Response:		FR				
0 ~ 20.0kHz				±0.2		dB
~ 40kHz (Note 9)				±0.3		dB

Note: 7. The passband and stopband frequencies scale with fs. For example, 20.02kHz at -0.02dB is 0.454 x fs.
The reference frequency of these responses is 1kHz.

8. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 24bit data of both channels on input register to the output of analog signal.

9. fs=96kHz.

DIGITAL CHARACTERISTICS

(Ta=25°C; VA, VD=4.75 ~ 5.25V; VT=2.7 ~ 5.25V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-100uA) (Note 10)	VOH	2.7 / VT-0.5	-	-	V
Low-Level Output Voltage (Iout=100uA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	uA

Note: 10. Min value is lower voltage of 2.7V or VT-0.4V.

SWITCHING CHARACTERISTICS

(Ta=25°C; VA, VD=4.75 ~ 5.25V, VT=2.7 ~ 5.25V; C_L=20pF)

Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
	Crystal Resonator	Frequency		11.2896		24.576	MHz
	External Clock	Frequency	fCLK	8.192		49.152	MHz
		Pulse Width Low	tCLKL	0.4/fCLK			ns
		Pulse Width High	tCLKH	0.4/fCLK			ns
CLKO Output (X'tal mode)		Frequency	fMCK	11.2896		24.576	MHz
		Duty Cycle	dMCK	35		65	%
LRCK Frequency							
Normal Speed Mode (DFS0="0", DFS1="0")			fsn	32		48	kHz
Double Speed Mode (DFS0="1", DFS1="0")			fsd	64		96	kHz
Quad Speed Mode (DFS0="0", DFS1="1")			fsq	128		192	kHz
	Duty Cycle	Slave mode		45		55	%
		Master mode			50		%
Audio Interface Timing							
	Slave mode						
	BICK Period		tBCK	81			ns
	BICK Pulse Width Low		tBCKL	33			ns
	Pulse Width High		tBCKH	33			ns
	LRCK Edge to BICK "↑" (Note 11)		tLRB	20			ns
	BICK "↑" to LRCK Edge (Note 11)		tBLR	20			ns
	LRCK to SDTO (MSB) (Except I^2S mode)		tLRS			40	ns
	BICK "↓" to SDTO		tBSD			40	ns
	SDTI Hold Time		tSDH	20			ns
	SDTI Setup Time		tSDS	20			ns
	Master mode						
	BICK Frequency		fBCK		64fs		Hz
	BICK Duty		dBCK		50		%
	BICK "↓" to LRCK		tMBLR	-20		20	ns
	BICK "↓" to SDTO		tBSD	-20		20	ns
	SDTI Hold Time		tSDH	20			ns
	SDTI Setup Time		tSDS	20			ns

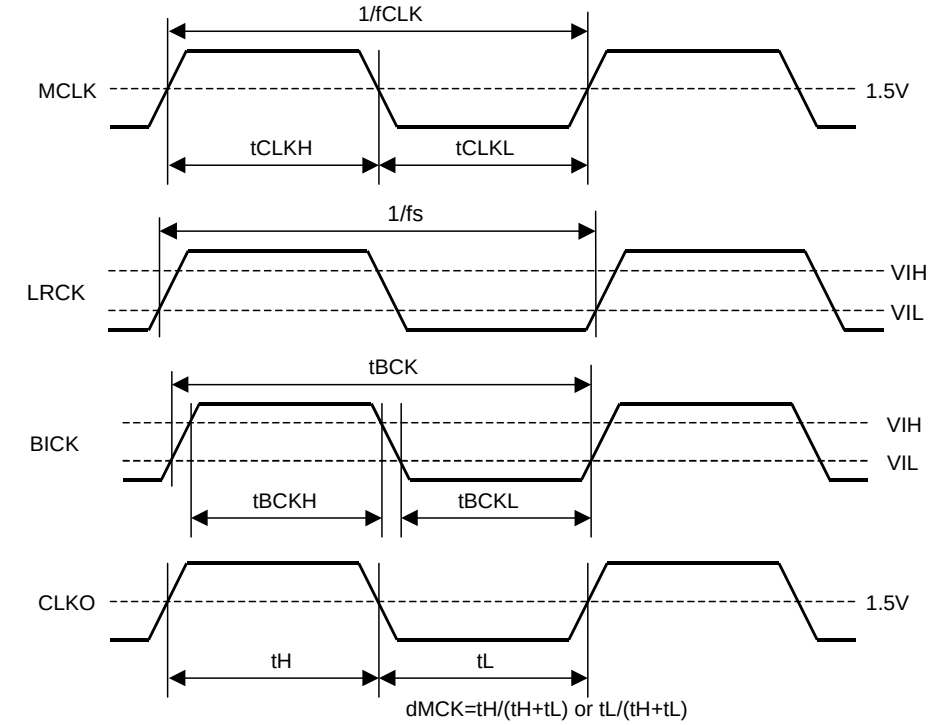
Note 11. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing					
CIF="0"					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CS "H" Time	tCSW	150			ns
CS "L" Time	tCSW	150			ns
CS "↑" to CCLK "↑"	tCSS	150			ns
CCLK "↑" to CS "↑"	tCSH	50			ns
CIF="1"					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CS "H" Time	tCSW	150			ns
CS "L" Time	tCSW	150			ns
CS "↓" to CCLK "↑"	tCSS	150			ns
CCLK "↑" to CS "↓"	tCSH	50			ns
Reset Timing					
$\overline{PD}$ Pulse Width (Note 12)	tPD	150			ns
RSTAD "↑" to SDTO valid (Note 13)	tPDV		516		1/fs

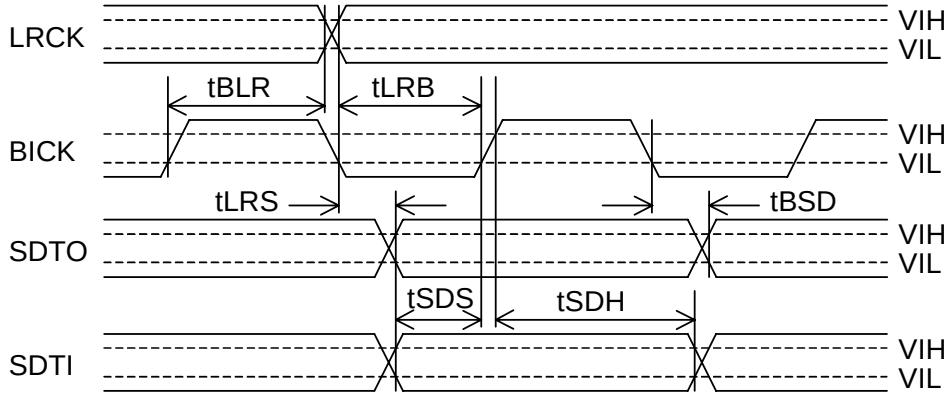
Note: 12. The AK4524 can be reset by bringing $\overline{PD}$ "L".

13. These cycles are the number of LRCK rising from RSTAD bit.

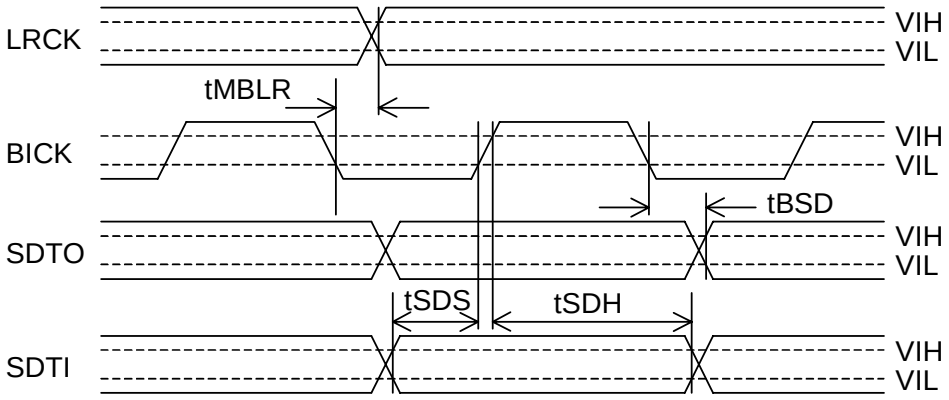
■ **Timing Diagram**



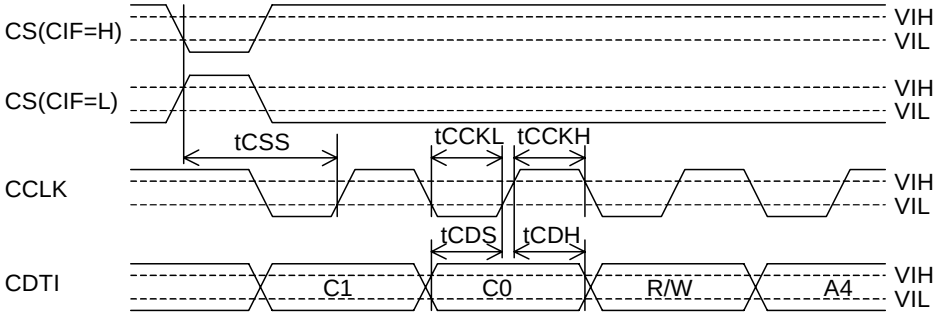
Clock Timing



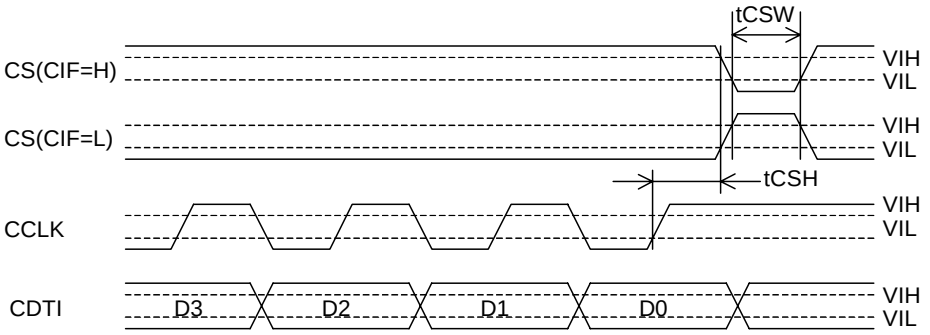
Audio Interface Timing (Slave mode)



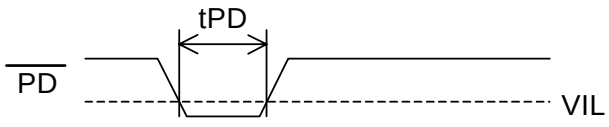
Audio Interface Timing (Master mode)



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The master clock (MCLK) can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. The master clock frequency can be selected by CMODE and CKS0-1 (Table 1). The sampling speed (normal speed mode, double speed mode or four times speed monitor mode) is selected by DFS0-1 (Table 2). The ADC is powered down during four times speed monitor mode. The frequency of the master clock output (CLKO) is the same as MCLK frequency and the output can be enabled or disabled by XTALE pin. When the CLKO output is not used externally, it should be disabled.

When using a crystal oscillator, external loading capacitors (between XTI/XTO and DGND) are required.

In slave mode, the LRCK clock input must be synchronized with MCLK, however the phase is not critical. Internal timing is synchronized to LRCK upon power-up. All external clocks must be present unless $\overline{PD}$ ="L" or all parts are powered down by control register, otherwise excessive current may result from abnormal operation of internal dynamic logic. In master mode, the clocks should be supplied by critical oscillation except for power down or the external clock (MCLK) should not be stopped.

CMODE	CKS1	CKS0	MCLK	
0	0	0	256fsn	at reset
0	0	1	512fsn	
0	1	0	1024fsn	
1	0	0	384fsn	
1	0	1	768fsn	

Table 1. Master clock frequency select
* fsn is a sampling rate at normal speed mode.

DFS1	DFS0	Sampling Rate		Monitor mode	
0	0	fsn	Normal speed	-	at reset
0	1	fsd=2 x fsn	Double speed	-	
1	0	fsq=4 x fsn	4 times speed (SDTO="L")	Simple Decimation	
1	1	fsq=4 x fsn	4 times speed (SDTO="L")	2 tap filter	

Table 2. Sampling speed

MCLK			Normal	Double	4 times
	fsn=44.1kHz	fsn=48kHz			
256fsn	11.2896MHz	12.288MHz	256fsn	N/A	N/A
512fsn	22.5792MHz	24.576MHz	512fsn	256fsd	128fsq
1024fsn	45.1584MHz	49.152MHz	1024fsn	512fsd	256fsq
384fsn	16.9344MHz	18.432MHz	384fsn	N/A	N/A
768fsn	33.8688MHz	36.864MHz	768fsn	384fsd	192fsq

Table 3. Master clock frequency
* X'tal mode operates from 11.2896MHz to 24.576MHz.
* The frequency over 24.576MHz supports only external clock mode.

■ Audio Serial Interface Format

Five serial modes selected by the DIF0 and DIF1 pins are supported as shown in Table 4. In all modes the serial data has MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. The interface supports both master mode and slave mode. In master mode, BICK and LRCK are outputs and the frequency of BICK is fixed to 64fs.

Mode	DIF2	DIF1	DIF0	SDTO	SDTI	LRCK	BICK	
0	0	0	0	24bit, MSB justified	16bit, LSB justified	H/L	≥ 32fs	
1	0	0	1	24bit, MSB justified	20bit, LSB justified	H/L	≥ 40fs	
2	0	1	0	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	at reset
3	0	1	1	24bit, IIS (I2S)	24bit, IIS (I2S)	L/H	≥ 48fs	
4	1	0	0	24bit, MSB justified	24bit, LSB justified	H/L	≥ 48fs	

Table 4. Audio data format

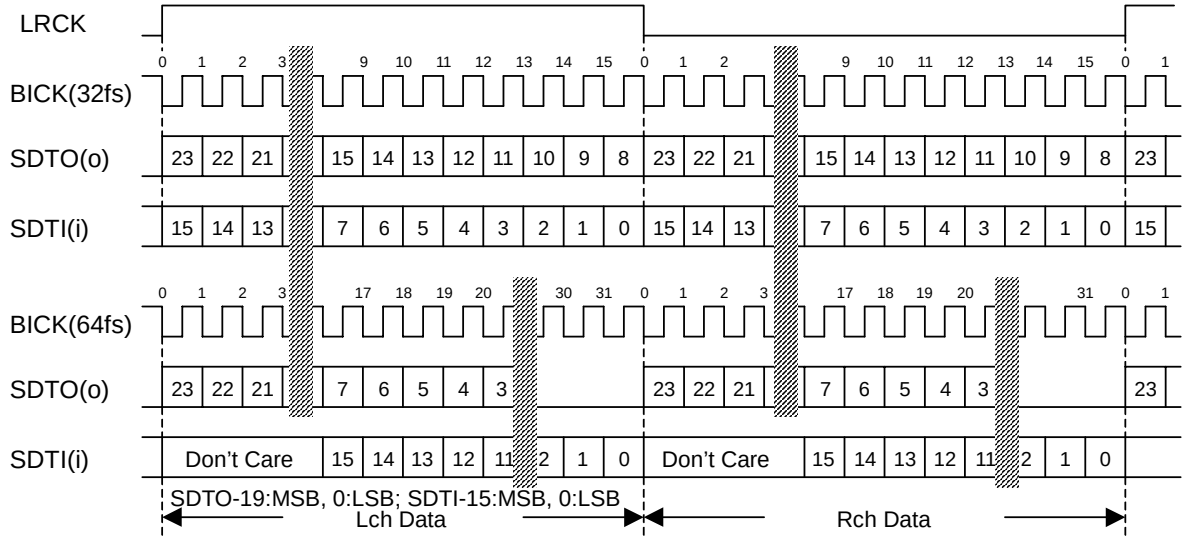


Figure 1. Mode 0 Timing

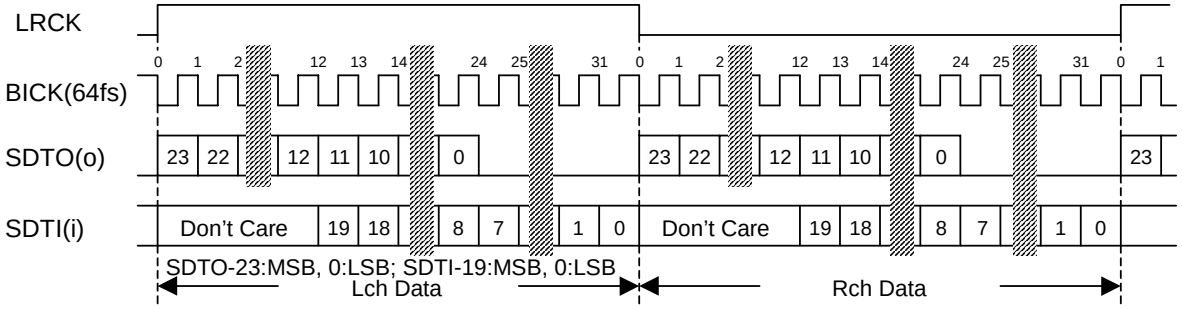


Figure 2. Mode 1 Timing

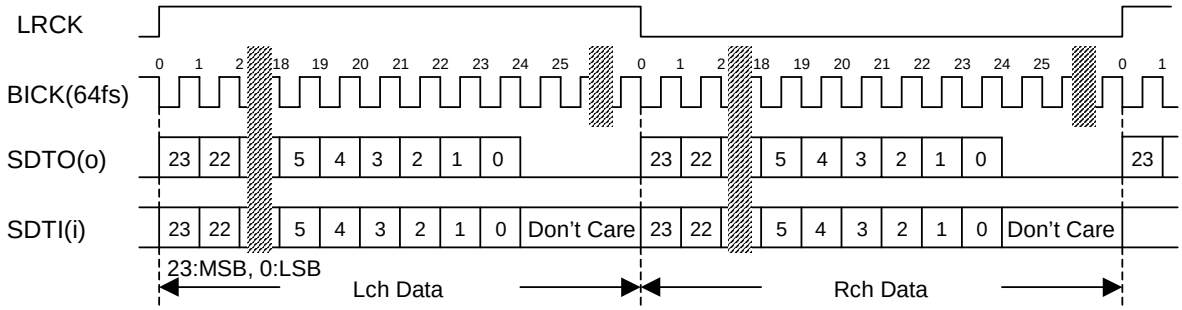


Figure 3. Mode 2 Timing

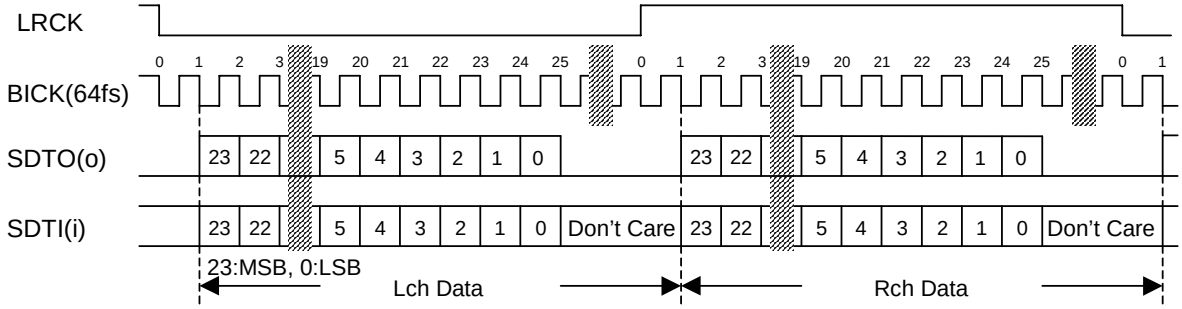


Figure 4. Mode 3 Timing

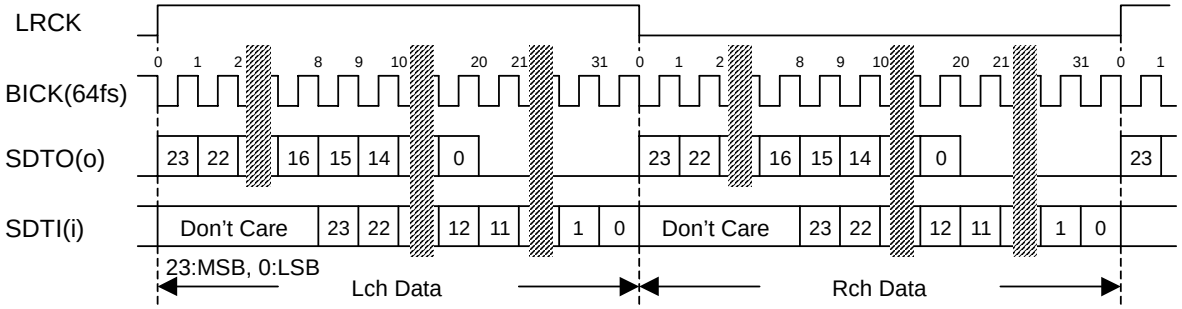


Figure 5. Mode 4 Timing

■ Input Volume

The AK4524 includes two channel independent analog volumes (IPGA) with 37 levels, 0.5dB step in front of ADC and digital volumes (IATT) with 128 levels (including MUTE) after ADC. The control data of both volumes are assigned in the same register address. When MSB of the register is "1", the IPGA changes and the IATT changes at MSB "0".

The IPGA is analog volumes and improves S/N compared with digital volume (Table 5). Level changes only occur during zero-crossings to minimize switching noise. Zero-crossing detection is performed channel independently. If there is no zero-crossings, then the level will change after a time-out. The time-out period (To) scales with fs. The periods of 256/fs, 512/fs, 1024/fs and 2048/fs are selectable by ZTM1-0 bits in normal speed mode. If new value is written to the IPGA register before IPGA changes by zero-crossing or time-out, the previous value becomes invalid. And then the timer (channel independent) for time-out is reset and the timer restarts for new IPGA value. Zero-crossing detection can be enabled by ZCEI in the control register.

The IATT is a pseudo-log volume linear-interpolated internally. When changing the level, the transition between ATT values has 8032 levels and is done by soft changes. Therefore, there is not any switching noise.

	Input Gain Setting		
	0dB	+6dB	+18dB
fs=44.1kHz, A-weight	100dB	98dB	90dB

Table 5. IPGA+ADC S/N

ZTM1	ZTM0	fsn	fsd	
0	0	256	512	
0	1	512	1024	
1	0	1024	2048	at reset
1	1	2048	4096	

Table 6. LRCK cycles for timeout period

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at fs=44.1kHz and also scales with sampling rate (fs).

■ Output Volume

The Ak4524 includes digital volumes (OATT) with 128 levels (including MUTE) which have the same architecture as IATT's in front of DAC. T he OATT is a pseudo-log volume linear-interpolated internally. When changing the level, the transition between ATT values has 8032 levels and is done by soft changes. Therefore, there is not any switching noise.

■ De-emphasis Filter

The DAC includes the digital de-emphasis filter (tc=50/15us) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). This setting is done via contorl register. This filter is always OFF at double speed and four times speed modes.

No	DEM1	DEM0	Mode	
0	0	0	44.1kHz	
1	0	1	OFF	at reset
2	1	0	48kHz	
3	1	1	32kHz	

Table 7. De-emphasis control (DFS0=DFS1="0")

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When SMUTE goes "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

Soft mute function is independent to output volume and cascade connected between both functions.

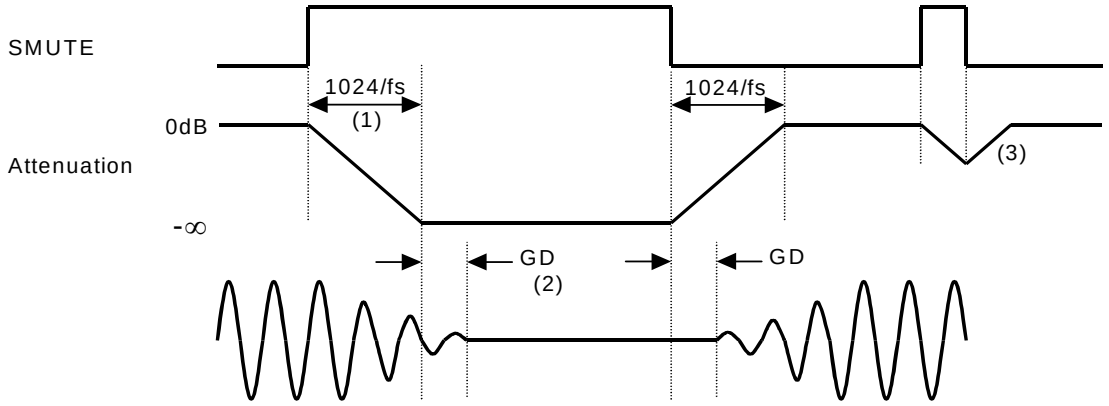


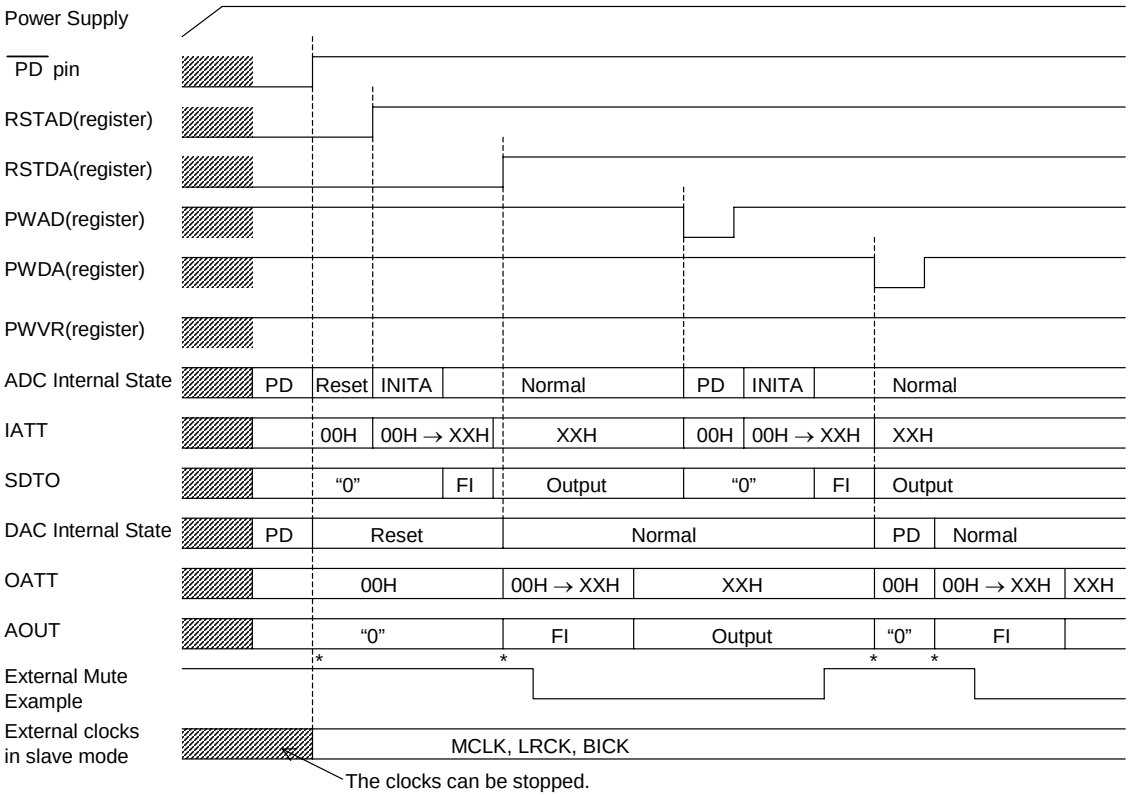
Figure 6. Soft Mute

Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

■ Power Down & Reset

The ADC and DAC of AK4524 are placed in the power-down mode by bringing a power down pin, $\overline{PD}$ "L" and each digital filter is also reset at the same time. The internal register values are initialized by $\overline{PD}$ "L". This reset should always be done after power-up. And then as both control registers of ADC and DAC go reset state (RSTAD=RSTDA="0"), each register sholud be cancelled after doing the needed setting. In case of the ADC, an analog initialization cycle starts after exiting the power-down or reset state. Therefore, the output data, SDTO becomes available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Power down mode can be also controlled by the registers (PWAD, PWDA).



- INITA: Initializing period of ADC analog section (516/fs).
- PD: Power down state. The contents of all registers are hold.
- XXH: The current value in ATT register.
- FI: Fade in. After exiting power down and reset state, ATT value fades in.
- AOUT: Some pop noise may occur at "*".

Figure 7. Reset & Power down sequence

■ Relationship between Clock Operation and Power-Down

XTALE pin controls the clock outputs. The operation in slave mode is shown Table 8. Table 9 shows the master mode operation. When a crystal oscillator is used, XTALE pin is set to "H". XTALE pin should be "L" at external clock mode.

Slave Mode	XTALE=L		XTALE=H	
	$\overline{PD}$ =H	$\overline{PD}$ =L	$\overline{PD}$ =H	$\overline{PD}$ =L
XTAL mode	Inhibit	Inhibit	Normal operation XTAL = Oscillation CLKO = Output LRCK = Input BICK = Input	Power down XTAL = Oscillation CLKO = Output LRCK = Input BICK = Input
EXT Clock mode	Normal operation XTI = MCLK in XTO = L CLKO = L LRCK = Input BICK = Input	Shut off XTI = MCLK in XTO = L CLKO = L LRCK = Input BICK = Input	Inhibit	Inhibit

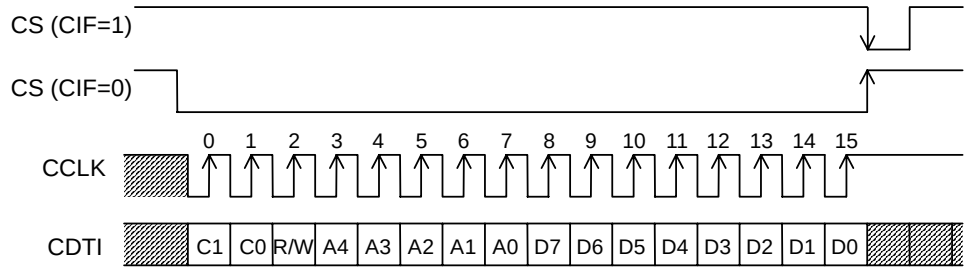
Table 8. Clock operation at slave mode (M/$\overline{S}$ = L)

Master Mode	XTALE=L		XTALE=H	
	$\overline{PD}$ =H	$\overline{PD}$ =L	$\overline{PD}$ =H	$\overline{PD}$ =L
XTAL mode	Inhibit	Inhibit	Normal operation XTAL = Oscillation CLKO = Output LRCK = Output BICK = Output	Power down XTAL = Oscillation CLKO = Output LRCK = H BICK = L
EXT Clock mode	Normal operation XTI = MCLK in XTO = L CLKO = L LRCK = Output BICK = Output	Shut off XTI = MCLK in XTO = L CLKO = L LRCK = H BICK = L	Inhibit	Inhibit

Table 9. Clock operation at master mode (M/$\overline{S}$ = H)

■ Serial Control Interface

The internal registers are written by the 3 wire uP interface pins: CS, CCLK, CDTI. The data on this interface consists of Chip address (2bits, C0/1) Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK. Data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CS. The operation of the control serial port may be completely asynchronous with the audio sample rate. The maximum clock speed of the CCLK is 5MHz. The CS should be "H" or "L" if no access. The chip address is fixed to "10". Writing is invalid for the access to the chip address except for "10". $\overline{PD}$ = "L" resets the registers to their default values.



C1-C0: Chip Address (Fixed to "10")
R/W: READ/WRITE (Fixed to "1":WRITE)
A4-A0: Register Address
D7-D0: Control data

Figure 8. Control I/F Timing

* READ command is not supported.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	0	0	0	0	0	PWVR	PWAD	PEDA
01H	Reset Control	0	0	0	0	0	0	RSTAD	RSTDA
02H	Clock and Format Control	DIF2	DIF1	DIF0	CMODE	CKS1	CKS0	DFS1	DFS0
03H	Deem and Volume Control	SMUTE	0	0	ZCEI	ZTM1	ZTM0	DEM1	DEM0
04H	Lch IPGA Control	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
05H	Rch IPGA Control	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
06H	Lch ATT Control	0	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
07H	Rch ATT Control	0	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0

Note: For addresses from 08H to 1FH, data is not written.
$\overline{PD}$ = "L" resets the registers to their default values.

■ Control Register Setup Sequence

When $\overline{PD}$ pin goes "L" to "H" upon power-up etc., the AK4524 should operate by the next sequence. In this case, all control registers are set to initial values and the AK4524 is in the reset state.

(1) Set the clock mode and the audio data interface mode.
(2) Cancel the reset state by setting RSTAD or RSTDA to "1". Refer to Reset Contorl Register (01H).
(3) ADC outputs and DAC outputs should be muted externally until cancelling each reset state. In master mode, there is a possibility the frequency and duty of LRCK and BICK outputs become an abnormal state.

The clock mode should be changed after setting RSTAD and RSTDA to "0". At that time, ADC outputs and DAC outputs should be muted externally. In master mode, there is a possibility the frequency and duty of LRCK and BICK outputs become an abnormal state.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	0	0	0	0	0	PWVR	PWAD	PWDA
	RESET	0	0	0	0	0	1	1	1

PWDA: DAC power down
0: Power down
1: Power up
Only DAC section is powered down by "0" and then the AOUTs go Hi-Z immediately. The OATTs also go "00H". But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the OATTs fade in the setting value of the control register (06H & 07H). The analog outputs should be muted externally as some pop noise may occur when entering to and exiting from this mode.

PWAD: ADC power down
0: Power down
1: Power up
Only ADC section is powered down by "0" and then the SDTO goes "L" immediately. The IPGAs also go "00H". But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the IPGAs fade in the setting value of the control register (04H & 05H). At that time, ADCs output "0" during first 516 LRCK cycles.

PWVR: Vref power down
0: Power down
1: Power up
All sections are powered down by "0" and then both ADC and DAC do not operate. The contents of all register are not initialized and enabled to write to the registers. When PWAD and PWDA go "0" and PWVR goes "1", only VREF section can be powered up.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Reset Control	0	0	0	0	0	0	RSTAD	RSTDA
	RESET	0	0	0	0	0	0	0	0

RSTDA: DAC reset

0: Reset

1: Normal Operation

The internal timing is reset by "0" and then the AOUTs go VCOM voltage immediately. The OATTs also go "00H". But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the OATTs fade in the setting value of the control register (06H & 07H). The analog outputs should be muted externally as some pop noise may occur when entering to and exiting from this mode.

RSTDA: ADC reset

0: Reset

1: Normal Operation

The internal timing is reset by "0" and then SDTO goes "L" immediately. The IPGAs also go "00H". But the contents of all register are not initialized and enabled to write to the register. After exiting the power down mode, the IPGAs fade in the setting value of the control register (04H & 05H). At that time, ADCs output "0" during first 516 LRCK cycles.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock and Format Control	DIF2	DIF1	DIF0	CMODE	CKS1	CKS0	DFS1	DFS0
	RESET	0	1	0	0	0	0	0	0

DFS1-0: Sampling Speed Control (see Table 2)

Initial: Normal speed

CMODE, CKS1-0: Master Clock Frequency Select (see Table 1)

Initial: 256fs

DIF2-0: Audio data interface modes (see Table 4)

000: Mode 0

001: Mode 1

010: Mode 2

011: Mode 3

100: Mode 4

Initial: 24bit MSB justified for both ADC and DAC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Deem and Volume Control	SMUTE	0	0	ZCEI	ZTM1	ZTM0	DEM1	DEM0
RESET		0	0	0	1	1	0	0	1

DEM1-0: De-emphasis response (see Table 7)
00: 44.1kHz
01: OFF
10: 48kHz
11: 32kHz
Initial: OFF

ZTM1-0: Zero crossing time out period select (see Table 6)
Initial: 1024fs

ZCEI: ADC IPGA Zero crossing enable
0: Input PGA gain changes occur immediately
1: Input PGA gain changes occur only on zero-crossing or after timeout.
Initial: 1 (Enable)

SMUTE: DAC Input Soft Mute control
0: Normal operation
1: DAC outputs soft-muted
The soft mute is independent of the output ATT and performed digitally.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch IPGA Control	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
05H	Rch IPGA Control	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
RESET		0	1	1	1	1	1	1	1

IPGL/R7-0: ADC Input Gain Level
Refer to Table 10
Initial: 7FH (0dB)

Digital ATT with 128 levels operates when writing data of less than 7FH. This ATT is a linear ATT with 8032 levels internally and these levels are assigned to pseudo-log data with 128 levels. The transition between ATT values has 8032 levels and is done by soft changes. For example, when ATT changes from 127 to 126, the internal ATT value decreases from 8031 to 7775 one by one every fs cycles. It takes 8031 cycles (182ms@fs=44.1kHz) from 127 to 0 (Mute).

The IPGAs are set to "00H" when $\overline{PD}$ pin goes "L". After returning to "H", the IPGAs fade in the initial value, "7FH" by 8031 cycles.
The IPGAs are set to "00H" when PWAD goes "0". After returning to "1", the IPGAs fade in the current value. But the ADCs output "0" during first 516 cycles.
The IPAGs are set to "00H" when RSTAD goes "0". After returning to "1", the IPGAs fade in the current value. But the ADCs output "0" during first 516 cycles.

Data	Internal (DATT)	Gain (dB)	Step width (dB)	
255 - 165	-	+18	-	IPGA Analog volume with 0.5dB step
164	-	+18	-	
163	-	+17.5	0.5	
162	-	+17	0.5	
:	-	:	0.5	
130	-	+1.0	0.5	
129	-	+0.5	0.5	
128	-	0	0.5	
127	8031	0	-	IATT External 128 levels are converted to internal 8032 linear levels of DATT. Internal DATT soft-changes between DATAs. DATT=2^m x (2 x l + 33) – 33 m: MSB 3-bits of data l: LSB 4-bits of data
126	7775	-0.28	0.28	
125	7519	-0.57	0.29	
:	:	:	:	
112	4191	-5.65	0.51	
111	3999	-6.06	0.41	
110	3871	-6.34	0.28	
:	:	:	:	
96	2079	-11.74	0.52	
95	1983	-12.15	0.41	
94	1919	-12.43	0.28	
:	:	:	:	
79	1023	-17.90	0.53	
78	975	-18.32	0.42	
77	943	-18.61	0.29	
:	:	:	:	
64	495	-24.20	0.54	
63	471	-24.64	0.43	
62	455	-24.94	0.30	
:	:	:	:	
48	231	-30.82	0.58	
47	219	-31.29	0.46	
46	211	-31.61	0.32	
:	:	:	:	
32	99	-38.18	0.67	
31	93	-38.73	0.54	
30	89	-39.11	0.38	
:	:	:	:	
16	33	-47.73	0.99	
15	30	-48.55	0.83	
14	28	-49.15	0.60	
:	:	:	:	
5	10	-58.10	1.58	
4	8	-60.03	1.94	
3	6	-62.53	2.50	
2	4	-66.05	3.52	
1	2	-72.07	6.02	
0	0	MUTE		

Table 10. IPGA code table

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Lch OATT Control	0	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
07H	Rch OATT Control	0	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
RESET		0	1	1	1	1	1	1	1

ATTL/R6-0: DAC ATT Level

Refer to Table 11

Initial: 7FH (0dB)

The AK4524 includes digital ATT with 128 levels equivalent to ADC's.

The OATTs are set to "00H" when $\overline{PD}$ pin goes "L". After returning to "H", the OATTs fade in the initial value, "7FH" by 8031 cycles.

The OATTs are set to "00H" when PWDA goes "0". After returning to "1", the OATTs fade in the current value.

The OATTs are set to "00H" when RSTDA goes "0". Afer returning to "1", the OATTs fade in the current Value.

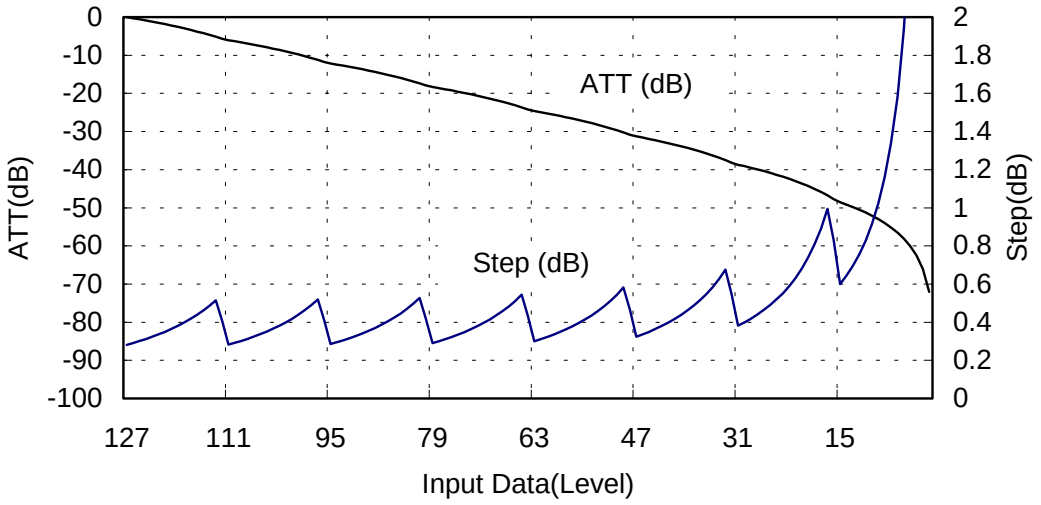


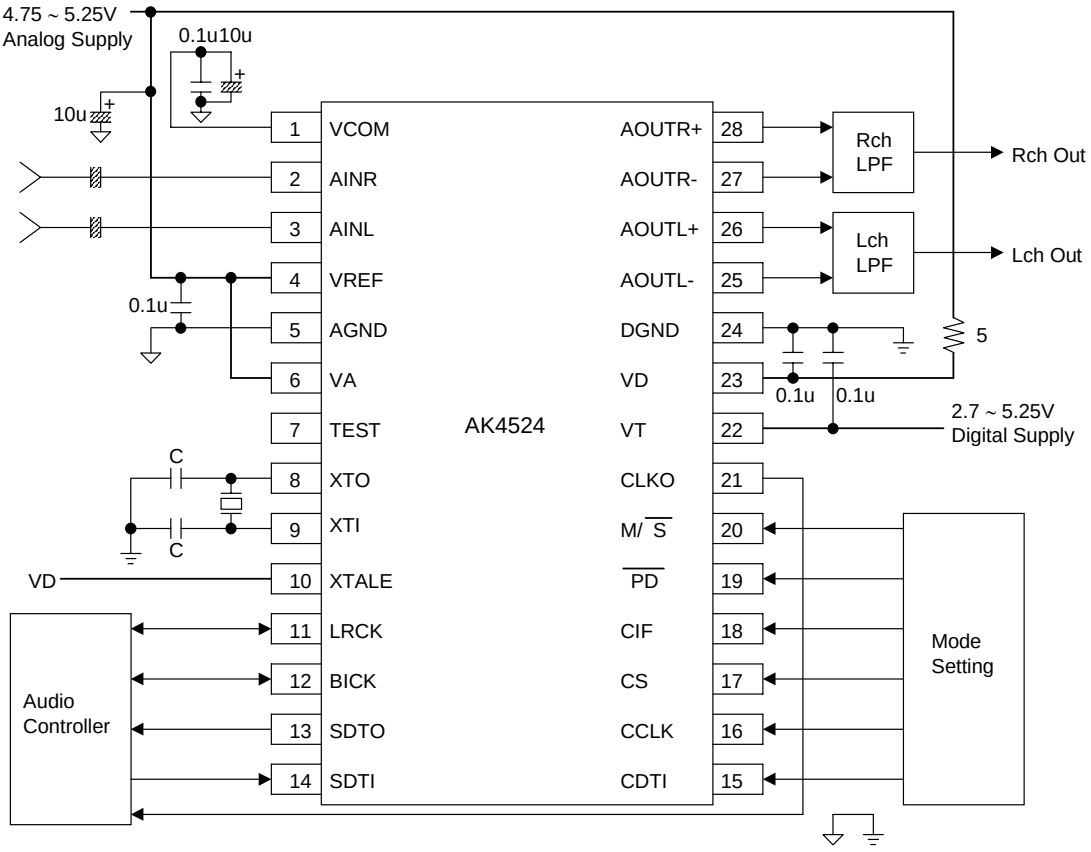
Figure 9. ATT characteristics

Data	Internal (DATT)	Gain (dB)	Step width (dB)	
127	8031	0	-	OATT External 128 levels are converted to internal 8032 linear levels of DATT. Internal DATT soft-changes between DATAs. DATT=2^m x (2 x l + 33) – 33 m: MSB 3-bits of data l: LSB 4-bits of data
126	7775	-0.28	0.28	
125	7519	-0.57	0.29	
:	:	:	:	
112	4191	-5.65	0.51	
111	3999	-6.06	0.41	
110	3871	-6.34	0.28	
:	:	:	:	
96	2079	-11.74	0.52	
95	1983	-12.15	0.41	
94	1919	-12.43	0.28	
:	:	:	:	
79	1023	-17.90	0.53	
78	975	-18.32	0.42	
77	943	-18.61	0.29	
:	:	:	:	
64	495	-24.20	0.54	
63	471	-24.64	0.43	
62	455	-24.94	0.30	
:	:	:	:	
48	231	-30.82	0.58	
47	219	-31.29	0.46	
46	211	-31.61	0.32	
:	:	:	:	
32	99	-38.18	0.67	
31	93	-38.73	0.54	
30	89	-39.11	0.38	
:	:	:	:	
16	33	-47.73	0.99	
15	30	-48.55	0.83	
14	28	-49.15	0.60	
:	:	:	:	
5	10	-58.10	1.58	
4	8	-60.03	1.94	
3	6	-62.53	2.50	
2	4	-66.05	3.52	
1	2	-72.07	6.02	
0	0	MUTE		

Table 11. OATT code table

SYSTEM DESIGN

Figure 10 & Figure 11 show the system connection diagram. This is an example which the AK4524 operates at X'tal mode. In case of external clock mode, please refer to Figure 11. An evaluation board (AKD4524) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Notes:

- X'tal Oscillation circuit is specified from 11.2896MHz to 24.576MHz.
- AGND and DGND of AK4524 should be distributed separately from the ground of external controller etc.
- When AOUT+/- drives some capcitive load, some resistor sholud be added in series between AOUT+/- and capacitive load.
- All input pins except pull-down pin (TEST) should not be left floating.

Figure 10. Typical Connection Diagram (X'tal mode)

X'tal Frequency	C
11.2896MHz, 12.288MHz	33pF
16.384MHz, 16.9344MHz, 18.432MHz	15pF
22.5792MHz, 24.576MHz	10pF

Table 12. External capacitance example for X'tal
(Please contact X'tal oscillator manufacturer)

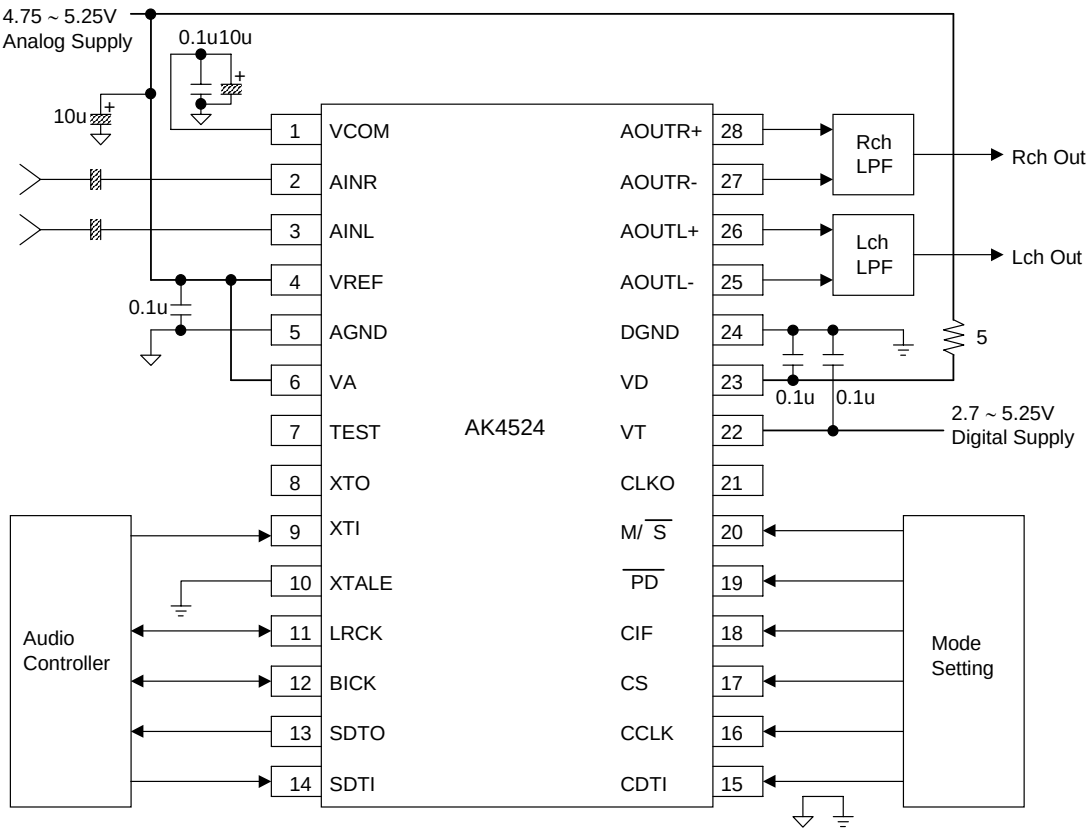


Figure 11. Typical Connection Diagram (EXT clock mode)

1. Grounding and Power Supply Decoupling

The AK4524 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is taken care. VT is a power supply pin to interface with the external ICs and is supplied from digital supply in system. AGND and DGND of the AK4524 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4524 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The differential voltage between VREF and AGND sets the analog input/output range. VREF pin is normally connected to VA with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4524.

3. Analog Inputs

The IPGA inputs are single-ended and the input resistance 5kΩ (min). The input signal range scales with the VREF voltage and nominally 0.58 x VREF Vpp centerd in the internal common voltage (about VA/2). Usually the input signal is AC coupled with capacitor. The cut-off frequency is fc=(1/2πRC). The AK4524 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative fill scale. The ideal code is 000000H(@24bit) with no input signal. The DC offset including ADC own DC offset removed by the internal HPF.

The AK4524 samples the analog inputs at 64fs. The digital filter rejects noise above the stopband except for multiples of 64fs. The AK4524 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

The analog outputs are full differential outputs and nominally 0.54 x VREF Vpp centered in the internal common voltage (about VA/2). The differential outputs are summed externally, Vout=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.4Vpp (typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal AOUT is 0V for 000000H(@24bit).

The internal switched-capacitor filter and the external LPF attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Differential outputs can eliminate any DC offset on analog outputs without using capacitors. Figure 12 to Figure 14 show the example of external op-amp circuit summing the differential outputs.

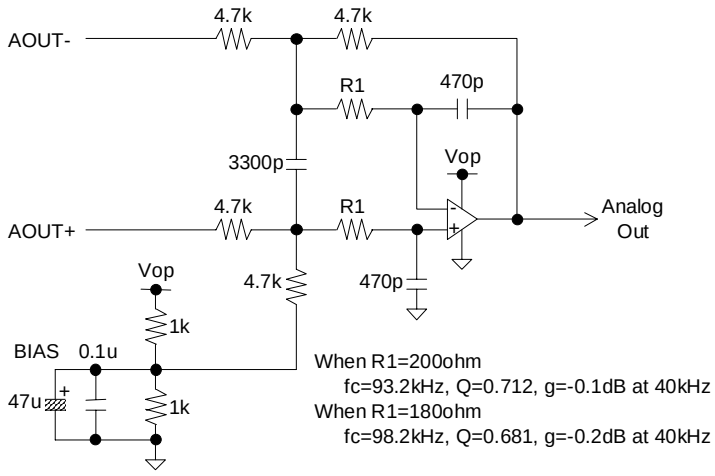


Figure 12. External 2nd order LPF Example (using single supply op-amp)

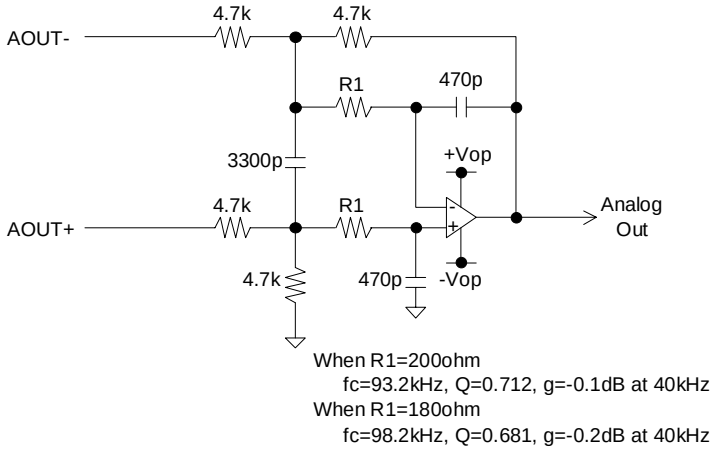


Figure 13. External 2nd order LPF Example (using dual supply op-amp)

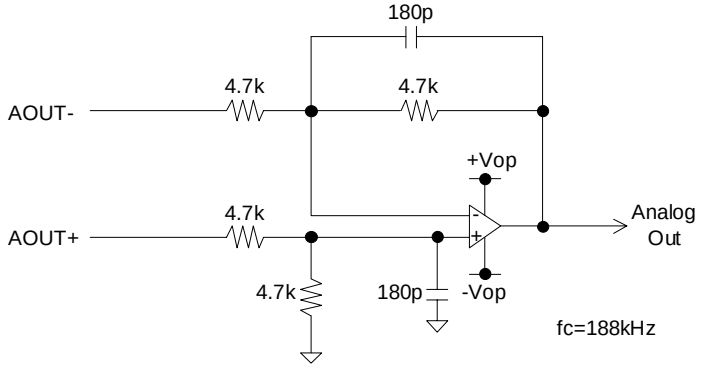


Figure 14. External low cost 1st order LPF Example (using dual supply op-amp)

■ Peripheral I/F Example

The digital inputs of the AK4524 are TTL inputs and can accept the signal of device with a nominal 3V supply. The digital output can interface with the peripheral device with a nominal 3V supply when the VT supply operates at a nominal 3V supply.

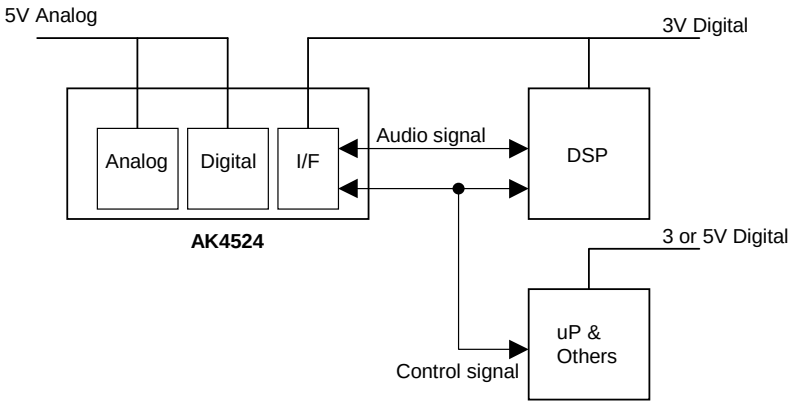
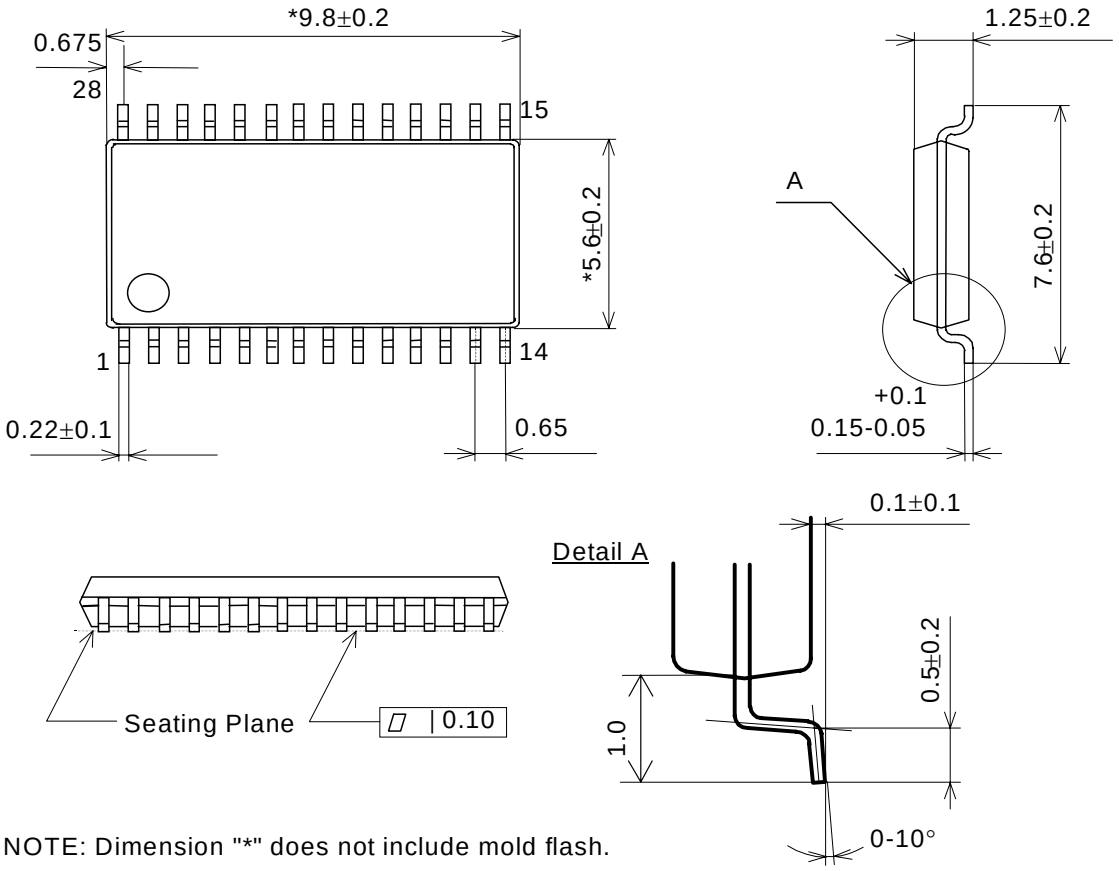


Figure 15. Power supply connection example

PACKAGE

28pin VSOP (Unit: mm)

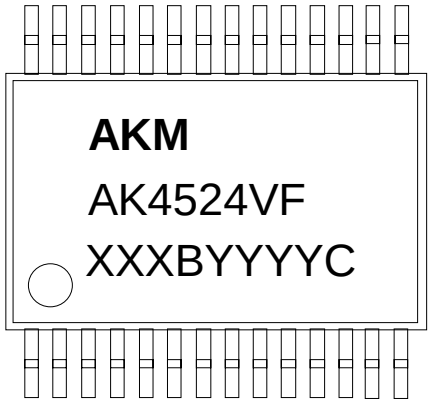


NOTE: Dimension "*" does not include mold flash.

■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



XXXBYYYYC: data code identifier

XXXB: Lot number (X: Digit number, B: Alpha character)
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

IMPORTANT NOTICE

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